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20 GHz GaAs MONOLITHIC POWER AMPLIFIER MODULE DEVELOPMENT
18 May 1984 - 17 May 1985

Prepared for

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16. Abstract

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Due to the success achieved during the first year of the program, most of the effort was spent on the direct common-source cascaded three-stage amplifier. After several modifications 1.8 W output power was obtained at 20 GHz with 10 dB gain and 14% efficiency. With reduced input power, 1.4 W was obtained with a linear gain of 13 dB. The amplifier was then redesigned to further improve microwave performance.

A four-stage lower power amplifier was also designed for use with the four-way traveling-wave combiner.

The output power of the distributed amplifier was increased to 0.8 W with 4 dB gain. This is higher than any distributed amplifier described in the literature.

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ANNUAL REPORT

FOR

CONTRACT NO. NAS3-23781

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EXECUTIVE SUMMARY

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SECTION I
INTRODUCTION

This report covers the second 12 months of a 36-month contract for the development of a 20 GHz GaAs FET monolithic power amplifier module for advanced communication applications. The objective of this program is to develop 20 GHz high power (2.5 W saturation, 1.5 W linear), high efficiency (20% at saturation), high gain (> 15 dB), wide bandwidth (19 to 21 GHz) monolithic GaAs FET amplifier modules for future satellite communication systems. The detailed requirements taken from the statement of work are given in Table 1.

Several amplifier design approaches have been pursued to accomplish the program goals. Four-way power combining of four 0.7 W amplifier modules was the original baseline approach. For this purpose, a monolithic four-way traveling-wave power divider/combiner was developed during the first year of the program. A distributed amplifier with six 300 μm gate width FETs and gate and drain transmission line tapers was also designed, fabricated, and evaluated for use as an 0.7 W module. This amplifier achieved an output power of 0.5 W with at least 4 dB gain across the entire 2 to 21 GHz frequency range during the first year of the program. Another approach is the direct common-source cascading of three power FET stages. An output power of up to 2 W with 12 dB gain and 20% power-added efficiency was achieved at 16.5 GHz with this approach during the first year of the program.

Because of its demonstrated performance, simplicity, smaller size, and higher efficiency, most of the effort during the second year of the program was concentrated on the direct common-source cascade approach. The work conducted on this approach during the last 12 months is described in Section II.A below.

As a backup approach the lower power four-stage monolithic amplifier developed under Contract NAS3-22886 was redesigned. This amplifier could be monolithically integrated with the traveling-wave combiner developed during the first year of the program to meet the program goals. The work on the four-stage monolithic amplifier is discussed in Section II.B.

Table 1

Objective Requirements of the 20 GHz GaAs FET Monolithic Power Amplifier Module

SOW Reference	
3.1.1	Electrical and rf Performance Objective Requirements
3.1.1.1	The GaAs FET Power Amplifier Module shall make maximum feasible use of monolithic technology to simultaneously optimize device gain, power, efficiency, and bandwidth.
3.1.1.2	rf Band: The rf band shall be from 19.0 to 21.0 GHz.
3.1.1.3	rf Output Power: The rf output power shall be greater than or equal to 2.5 W at saturation and 1.5 W linear (-20 dB 3rd order intermodulation products).
3.1.1.4	rf Gain: The rf gain shall be greater than or equal to 15 dB.
3.1.1.5	Gain Variation: The maximum gain shall not vary more than 1 dB over the entire 2.0 GHz bandwidth and 0.5 dB over any 500 MHz band.
3.1.1.6	Module Power Added Efficiency: The module power added efficiency shall be equal to or greater than 20% at saturation and 15% under linear operation (see 3.1.1.8).
3.1.1.7	Impedance: The nominal input and output impedance shall be 50 ohms. The input and output VSWR shall be less than or equal to 1.3:1.
3.1.1.8	Linearity: Third order intermodulation products shall be less than or equal to -20 dBc under linear operation.
3.1.1.9	Noise Figure: The noise figure at room temperature shall be less than or equal to 20 dB.
3.1.1.10	AM/PM Conversion: The AM/PM conversion shall not exceed 3°/dB.
3.1.1.11	Harmonic and Spurious Response: The harmonic response shall be at least -30 dBc. The spurious response shall be at least -60 dBc.

Table 1
(Continued)

SOW Reference	Electrical and rf Performance Objective Requirements
3.1.1.12	Maximum FET Channel Junction Temperature: The maximum FET channel junction temperature under worst case thermal conditions shall not exceed 110°C.
3.1.1.13	Module to Module Gain Variation: For any module, the gain at any given frequency in the bandwidth shall vary by no greater than ± 0.4 dB from the RMS average for all the modules at the given frequency.
3.1.1.14	Module to Module Phase Shift Variation: For any given module, the phase shift at any given frequency in the bandwidth shall vary by no greater than ± 10 degrees from the RMS average for all the modules at the given frequency.
3.1.1.15	Group Delay Variation: The group delay variation at and below saturation shall not exceed 0.5 ns over any 0.5 GHz portion of the operating frequency.

The distributed amplifier developed during the first year of the program was improved significantly during the second year by changing the materials structure as described in Section II.C. However, this approach is the least desirable of the three because, in addition to the large chip size of a circuit-level combining technique, it also has relatively low gain and efficiency.

In addition to the results described in Section II, technical achievements during this reporting period are summarized in Section III. Plans for the next period are given in Section IV.

SECTION II
SUBMODULE DEVELOPMENT

A. Three-Stage 2.5 W Amplifier

At the end of the first year of the program a three-stage monolithic amplifier had been designed and a number of slices fabricated. The best of these amplifiers produced 2 W output power with 12 dB gain and 20% efficiency in the 16 to 17 GHz range. The details of these results and the amplifier design were given in the first annual report. The goals for this second year of the program were to understand the reasons for the low frequency, to shift it to the 19 to 21 GHz band, and to improve gain and power to meet the program goals.

1. Amplifier Fabrication

Table 2 is a summary of all of the slices processed during the second year of the program. Both VPE and MBE slices were used and all were fabricated with the n^+ ledge channel structure. The best performance was obtained from the MBE slices as in the first year of the program. During the year, gate definition was shifted to the new CRL e-beam machine. Gate length variation and alignment accuracy is no longer a problem and all slices in Table 1 had 0.5 μm gate lengths.

There was a problem in lifting off the transmission line evaporated metal. This problem was in some way caused by the thin Cr layer in the metallization that is included as an RIE etch stop for the source pads, which are defined at the same time. The Cr causes some distortion in the resist profile, which is enough to prevent lift off of some pattern geometries such as the metal between narrow lines several hundred micrometers apart. There was no problem lifting off source/drain patterns which are only a few micrometers apart. The problem was temporarily solved by separating the transmission line and overlay metal evaporations and eliminating the Cr from the transmission lines since it serves no function there. This is not desirable, however, since an extra mask step and metal evaporation are required. The problem was solved by replacing the chlorobenzene-soaked resist lift off with a multilayer resist/Ge/resist lift off. This works because the multilayer structure has a larger undercut profile, but the

Table 2

Slices Completed During the Second Year of the Program

Slice Number	n ($\times 10^{17}$ cm^{-3})	300 μm FET Power at 15 GHz (6 dB Gain, V_{ds} = 8 V) (mW)	Amplifier Performance				Comments
			Gain (dB)	Power (W)	Freq. (GHz)	Yield (%)	
MBE-606	2.9	166	10	1.0	16-17	11	Low Breakdown Voltage
83E1-118	2.4	178	--	--	--	14	Oscillates
83E1-113	2.4	200	--	<1.0	16-17	1	Low Power Unexplained
MBE-624	3.4	216	10	1.6	16-17	3	
84E1-4	2.6	191	*	*	13	7	40% Thinner Nitride
MBE-653	2.8	224	9	1.6	19	22	37% Thicker Nitride
MBE-654	2.4	224	10	1.8	20	18	New Transmission Lines
MBE-651-65	2.3	214	9	1.5	20	2	New Transmission Lines
84E1-8	2.4	204				2	New Transmission Lines

*Mismatched

Note: All n^+/n slices
Gate lengths all ~ 0.5 μm
300 μm FET Gains all 10-11 dB at 15 GHz

extra Ge evaporation causes some delay. This process has now been superseded by a positive resist/PMMA process with deep-UV exposure of the PMMA to produce a large undercut. Now transmission lines and overlay metal can be defined together with no lift off problems.

Amplifier yield from the best slices was about 20% as seen in Table 2. This is an improvement over the first year and could have been ~ 50% but for a gold plating problem during air bridge plating. The plating solution undercut the defining resist coating and shorted some closely spaced patterns. The air bridge plating procedure has been changed somewhat to a process developed on another program that appears to be superior. One test slice did not have any plating problems, but several slices should be processed before it is certain that the difficulty has been eliminated.

The two highest yield slices (MBE-653 and MBE-654) also demonstrated the most uniform saturated currents ever observed at TI for any GaAs material. The improvement was obtained by increasing the size of the Ga effusion cell in the MBE machine. The slices had n^+ contact layers, n ~ 2.5 x 10^{17} cm^{-3} active layers, and undoped buffer layers. Following ohmic contact formation, the saturated current was measured on 60 of the 150 μm gate width test devices across one of the 2-inch slices. The mean current was 370 mA with a standard deviation of 2.4 mA = 0.65% of the mean. There was no radial dependence of this current. When two low points at one edge were omitted, the standard deviation dropped to 1.8 mA = 0.49% and all values were between 367 mA and 373 mA. Similar earlier slices typically had a drop of ~ 40 mA from the center to the edge. When gates were defined (with the n^+ ledge channel structure) on these slices, the process of recessing the gates did not appear to increase severely the variation of saturated current across the slices. Following gate definition, the standard deviation in I_{dss} was about 3 mA, which may be compared with about 2 mA following ohmic contact definition. The fractional variation is much larger, of course, since the absolute current values are much less now (about 50 mA instead of 370 mA for 150 μm gate width). The increased uniformity with these slices significantly improves amplifier yield because all FETs on the slice have I_{dss} within the usable range, compared with only 50% or less typically.

One of the slices in Table 2 (MBEϕ1-65) came from the new Perkin-Elmer MBE machine. The device microwave performance was as good as that of FETs from the older Riber machine, and the doping transition was even sharper (~300 Å/decade) than can be achieved with the Riber machine (~400 Å/decade). The uniformity is not yet quite as good as the best slices described above, but is certainly usable and further improvements are expected. The best slice from the Riber machine had a standard deviation in saturated drain current of 0.65% of the mean for a 2 inch slice, while the Perkin-Elmer machine produced about 1.8%.

2. Amplifier Design and Performance

A slice (84E1-4) of the three-stage amplifier module with a 40% thinner silicon nitride thickness for the interstage shunt matching capacitors was processed and rf evaluated. The result was rather disappointing. Instead of increasing the operation frequency as predicted, this amplifier had a gain peaked at around 13 to 14 GHz with a small signal gain of around 20 dB. However, the output power was only about 1 W. Further amplifier circuit optimization with all the parasitics taken into account revealed that, with similar transmission line lengths as are presently used, the matching capacitors actually should have been 30% smaller instead of larger.

Such a slice was fabricated (MBE-653) and device output power was as good as that of the FETs on the best previous slice. Microwave results show that the frequency of operation has been increased to the 18 to 21 GHz range. A two-stage (the first two stages) chip has achieved a small-signal gain of 10 dB across the 17 to 20 GHz range. Under large-signal operation, an output power of 1.3 W was obtained with 8 dB gain at 17.5 GHz. A three-stage amplifier achieved an output power of 1.6 W with 9 dB gain at 19 GHz. The output power is still 1 to 2 dB lower than expected, but demonstrates that lower shunt capacitance values are required for operation in the desired frequency band.

In order to understand the reasons for low output power, individual FETs were sawed from the monolithic amplifiers of slice MBE-653 and tested at 10 GHz and 15 GHz. The results are summarized in Table 3. The low gain of the 6 mm gate width FET relative to two side-by-side 2.4 mm FETs implies that

Table 3
FET Microwave Performance

Gate Width (mm)	Gain (P_{in} = 0.105 W/mm) V_{ds} = 8 V	
	10 GHz (dB)	15 GHz (dB)
0.3	--	7.4
1.2	8.8	6.7
2.4	8.1	6.0
6.0	6.4	3.0
2 x 2.4	7.2	4.3

a major part of the problem lies with the 6 mm FET itself. This is not unexpected since there are only seven via holes for the 6 mm device as compared with the 2.4 mm device which has five vias. The extra source-lead inductance per unit gate width results in a gain degradation, especially at high frequencies.

It was also thought that the interstage impedances were somewhat mismatched, so, before the FETs were redesigned, the interstage transmission line characteristic impedances were reduced to verify that this was indeed the case. It was known from the high input and output return loss that the input and output impedances were already well matched. The change was simple, since it only required changing one coarse-geometry photomask. The last three slices in Table 1 were processed with this revised transmission line mask along with the thicker capacitor dielectric. Figure 1 is a photograph of a three-stage amplifier on one of these slices. The modifications may be seen by comparing this photograph with Figure 21 in the First Annual Report. The output lines on the first-stage FET were reduced in length and the input lines to the second- and third-stage FETs were reduced in impedance. The silicon nitride was made ~ 35% thicker to shift the operating frequency into the desired band.

FETs were tested at 15 GHz and the output power of the devices from the two MBE slices was found to be as good as the best previous devices. The small signal gain was about 0.5 dB higher than the best previous devices. FETs from the VPE slice had about 0.5 dB lower gain and power, but were still very good.

The transmission line modifications, as expected, had the effect of moving the operating frequency band into the 19 GHz to 21 GHz frequency range. Figure 2 shows the gain (output power)-frequency response of one of the amplifiers evaluated. At 20 GHz the output power was 1.8 W with a gain of 10.2 dB. The power-added efficiency was 14%. As can be seen, the 1 dB bandwidth covers almost the entire design bandwidth. With a reduced input rf drive, an output power of 1.4 W with a linear gain of 13 dB was obtained. These results approach the program goal of 1.5 W with a linear gain of 15 dB.

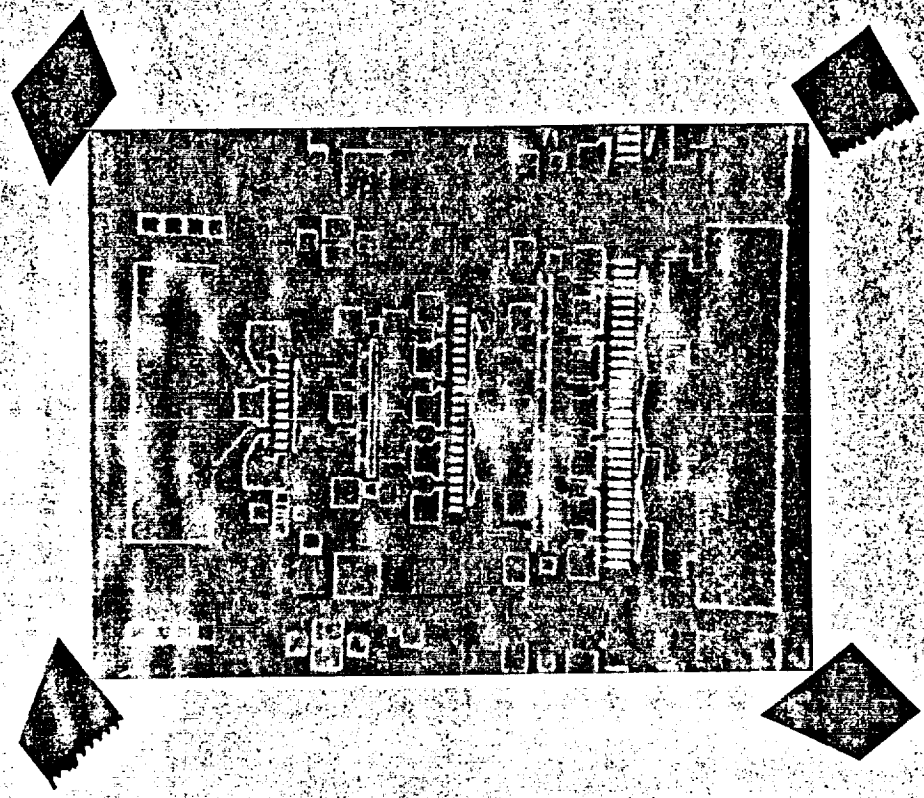


Figure 1. Photograph of Three-Stage Monolithic Amplifier Having Modified Terminations for Lines

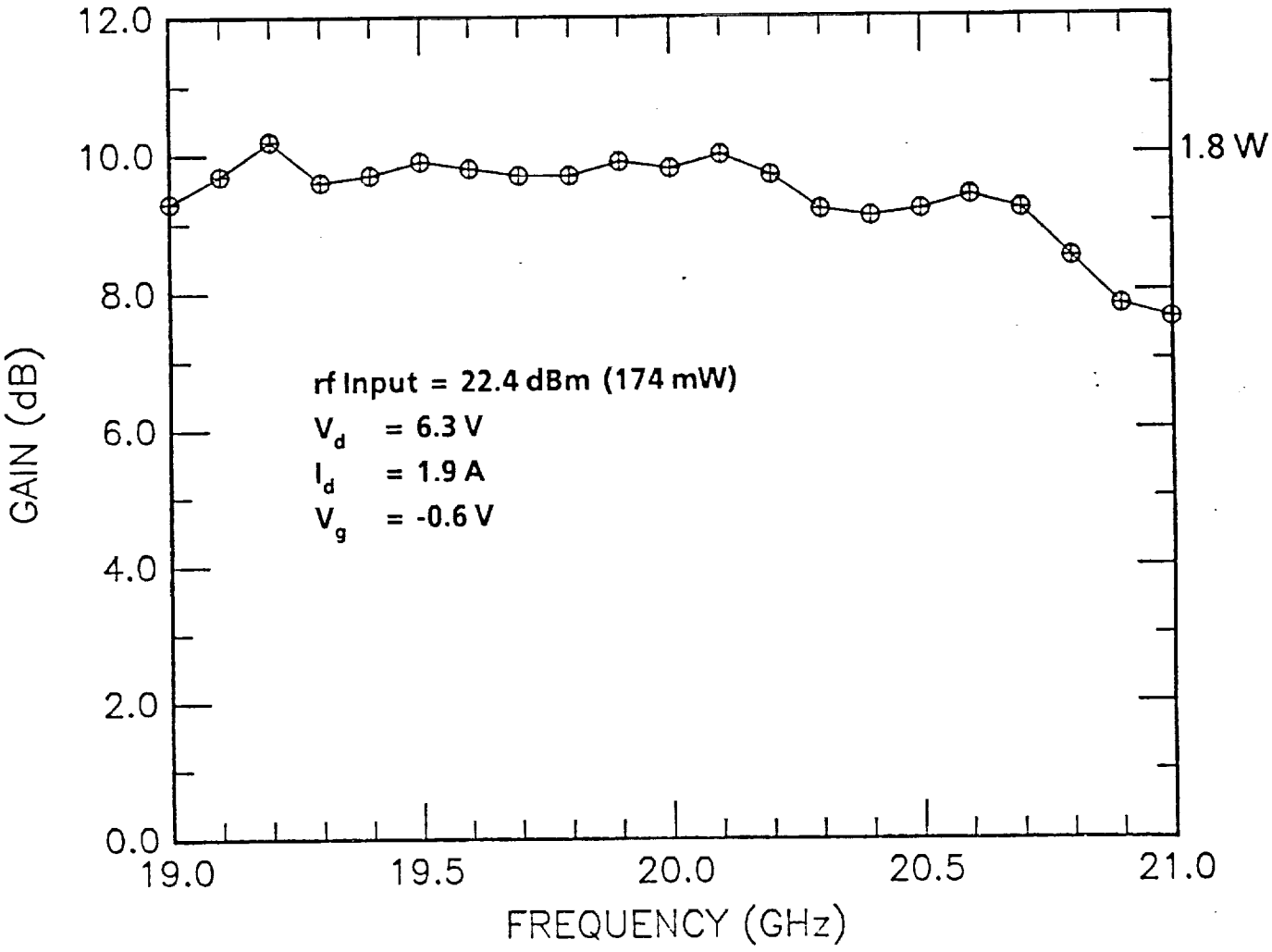


Figure 2 Gain-Frequency Response of a Three-Stage Amplifier

Following the achievement of the above results, the amplifier was redesigned to improve microwave performance so that all program goals could be met or exceeded. The FET gate widths remain the same, but via size is increased and extra vias are incorporated on the drain sides of the FETs to further reduce source lead inductances and increase gain. The transmission line lengths that gave the successful 19 to 21 GHz operation described above are retained. The matching capacitor areas are reduced so that the optimum silicon nitride thickness can be reduced back to 4000 Å from the 5500 Å used recently. The bias network is incorporated on the chip, which increases chip size from 3.3 mm x 2.0 mm to 4.0 mm x 3.0 mm. This will improve stability and greatly simplify bonding. The thin film resistors in the bias network require an additional mask level and mesa isolation is replaced by implantation isolation.

We have recently received the photomasks for the redesigned three-stage, 2.5 W monolithic amplifier. Figure 3 shows the digitized mask design data for this amplifier. The input is on the left, followed by 1200 μm, 2400 μm, and 6000 μm gate width FETs. Processing has begun on one slice to determine if there are any mask errors.

B. Four-Stage 0.7 W Amplifier

The four-stage amplifier developed under NASA Contract No. NAS3-22886 was redesigned for use with the four-way traveling-wave combiner as an alternative method for meeting the program goals. The FET gate widths are 300 μm, 300 μm, 600 μm and 1500 μm. This should produce an output power of about 0.7 W with at least 20 dB gain at 20 GHz. After the required performance is achieved, a new mask set will be designed (if necessary) incorporating four of these amplifiers with the traveling-wave divider/combiner already developed. In this redesign the FET performance has been improved by changing the geometry to source overlay with via grounding. The vias are twice as large as on the earlier three-stage, high-power amplifier submodule, and an extra via is included on the drain side of the output stage FET to further reduce source lead inductance. Gate and drain bias networks have also been incorporated on-chip to simplify bonding and eliminate the tendency for low-frequency bias-line oscillations. The bypass capacitors are 10 pF. Their size was reduced by reducing the silicon nitride

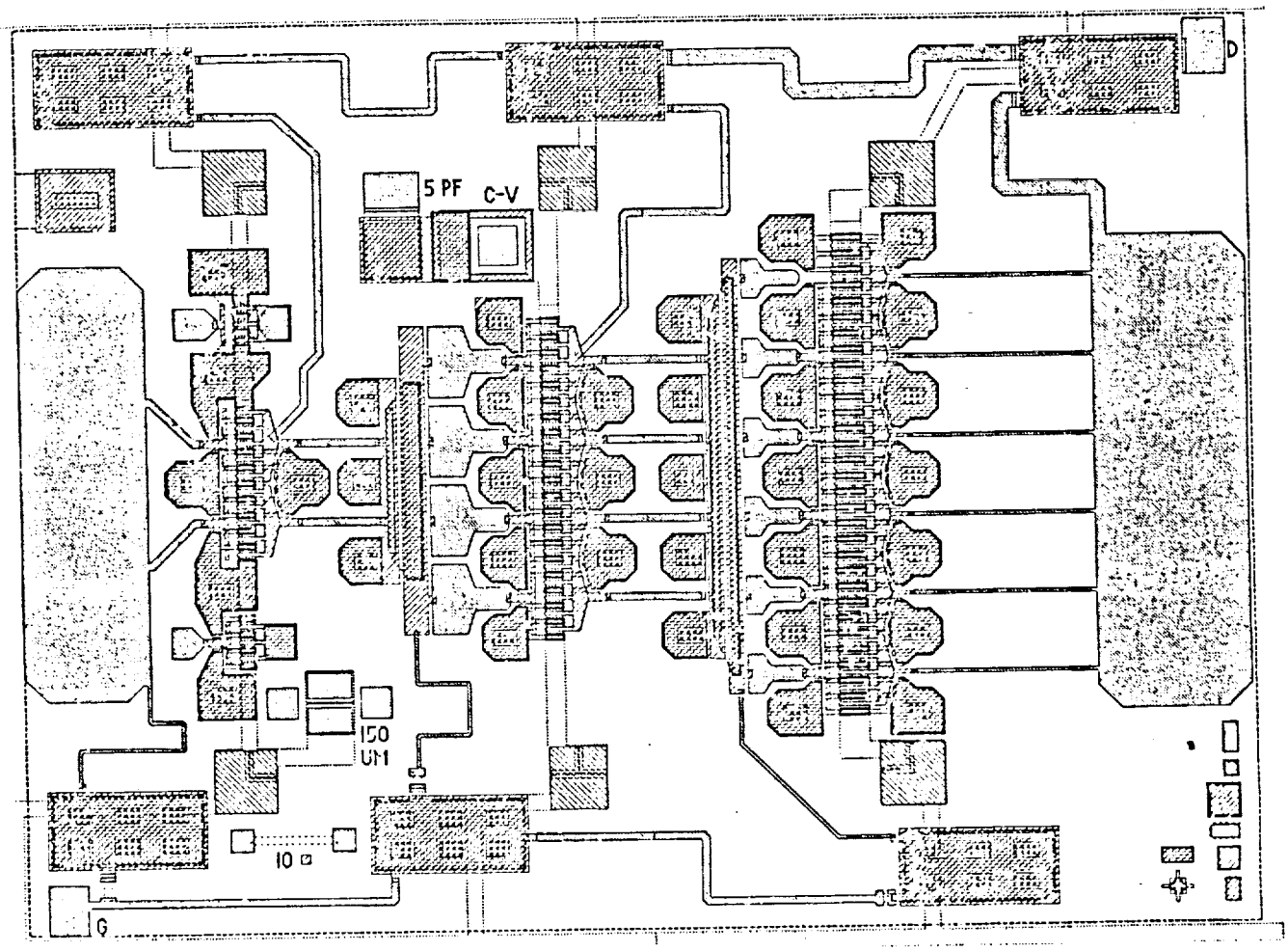


Figure 3 Digitized Design Data for Three-Stage Monolithic Amplifier

dielectric thickness to 2000 Å from the 4000 Å used on the three-stage amplifier. The chip length is 4.7 mm, and the width is only 1.2 mm, so that it exactly fits the divider/combiner. The fabrication process will be identical to that used for the present three-stage amplifier, except for the use of implantation isolation instead of mesa etching and the addition of an extra mask level to define thin film resistors in the bias network.

The advantage of this approach is that the output FETs (1.5 mm gate width) are much smaller than the output FETs of the three-stage directly cascaded amplifier (6 mm gate width). This reduces gain degradation due to excessive source lead inductance per unit gate width, phase variation across the FET, and difficulty in matching the very low FET input impedance. The disadvantage is the considerably larger chip size. The photomasks were recently received for the four-stage amplifier and Figure 4 shows the digitized mask design data. The input is on the left, followed by 300 μm, 300 μm, 600 μm, and 1500 μm gate width FETs. All bias and matching circuitry is integrated on the chip. Processing has begun on two slices that have implanted active layers. One will be processed with a new technique (developed on an internal program) for producing the n^+ ledge channel structure with a single e-beam lithography step. This will be the first time we have used this process other than on experiments with discrete FETs. Once we have verified there are no mask errors, n^+/n MBE slices will be used.

C. Distributed Amplifier

Device structure optimization of a distributed amplifier has been continued. The breakdown of an FET occurs at the drain side edge of a gate and it limits the output power of a distributed amplifier. The voltage has been improved by using MBE grown material with two active layers: n^- gate buffer layer ($1 \times 10^{17}/cm^3$) followed by an n active layer ($5 \times 10^{17}/cm^3$). The layer thicknesses were 0.2 μm and 0.05 μm, respectively. The usual buffer layer was provided under the n layer. To reduce the parasitic resistances, an n^+ contact layer was grown on top of the n^- layer. The material structure is depicted in Figure 5. The dc characteristics of a 75 μm wide FET based on the material is shown in Figure 6: g_m is 12 mmhos, and breakdown voltage is about 17 V (much better than the usual MESFET with a similar g_m, whose breakdown voltage is about 10 to 12 volts). The higher

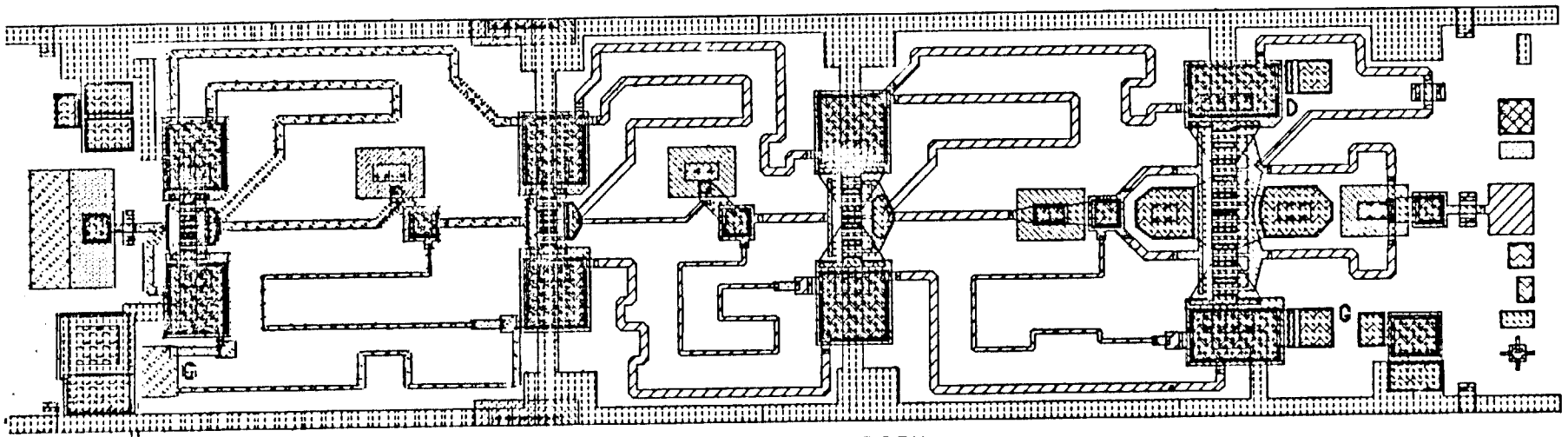


Figure 4 Digitized Design Data for Four-Stage Monolithic Amplifier

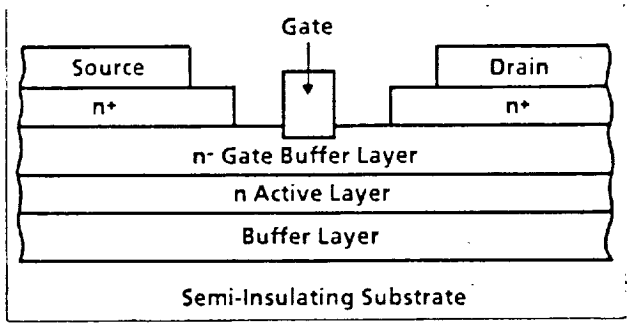
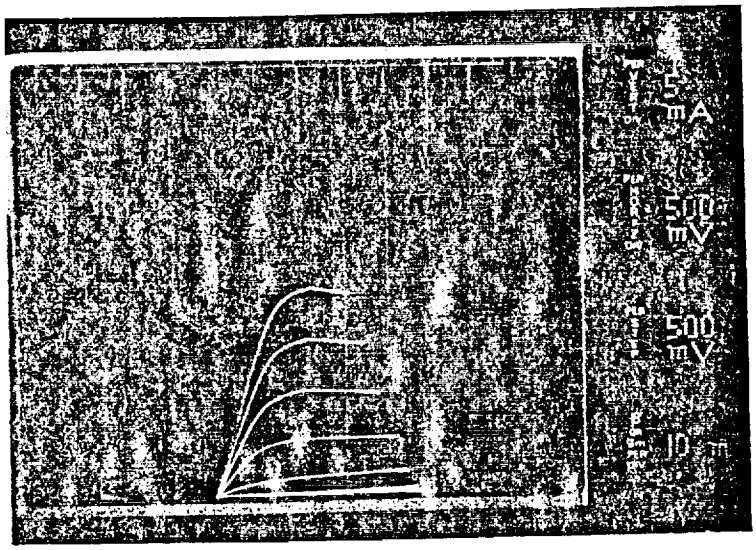
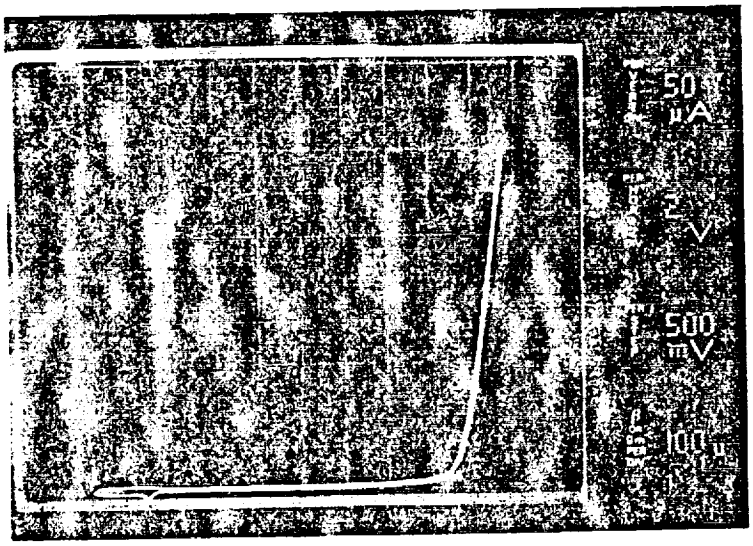


Figure 5 n^+ Ledge, Gate Buffer Layer Channel Structure



I-V CURVE



GATE-DRAIN BREAKDOWN

Figure 6 Dc Characteristics of an FET Built on Low-High Doped Material

breakdown voltage improved the power performance of the distributed amplifier. Over the 16 to 20 GHz frequency range a linear gain of 5 dB with an output power of 630 mW was obtained. Increased rf drive produced an output power of 800 mW with 4 dB gain and 15% power-added efficiency. The output power was about 2 dB above the best distributed amplifier using a flat doping profile (500 mW, 4 dB gain). The concept of using a low-high doping profile to improve device performance has thus been proved.

SECTION III
SUMMARY

Achievements in this program during the second 12 month period are summarized as follows:

- A three-stage directly cascaded amplifier produced 1.8 W output power with 10 dB gain and 14% efficiency at 20 GHz.
- A distributed amplifier with the gate buffer layer structure produced 800 mW output power with 4 dB gain and 15% efficiency.
- New MBE and e-beam machines were successfully brought on-line.
- Processing improvements have led to higher chip yields.
- The three-stage directly cascaded amplifier was redesigned to improve FET performance and incorporate on-chip bias networks.
- A four-stage lower power amplifier to be employed with a four-way traveling-wave combiner was designed as a backup approach.

SECTION IV
PLANS

- Fabricate redesigned three-stage directly-cascaded amplifiers on MBE material to meet or exceed all program goals.

- Revise transmission line mask and/or capacitor dielectric thickness on three-stage amplifier if necessary.

- Make all necessary rf measurements on completed amplifiers.

- Fabricate four-stage monolithic amplifiers and verify performance.

- Hybrid combine four-stage amplifiers with four-way traveling-wave combiner to check performance.

- Design new monolithic chip incorporating four-stage amplifiers and four-way combiners if three-stage amplifier cannot meet program goals.